

Product Features

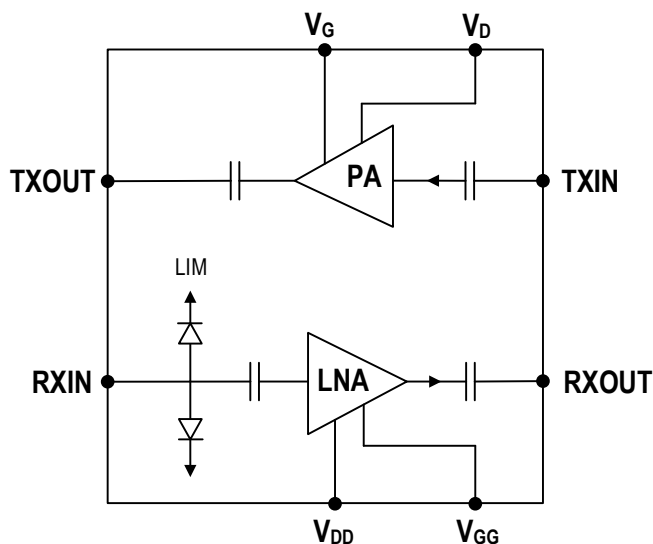
- Frequency Range: 8.0-11 GHz
- RX Noise Figure: 1.61 dB
- RX small Signal Gain: 26.5 dB
- RX Output TOI: 20 dBm
- TX Large Signal Gain: 24.1 dB
- TX Saturated Power: 42.2 dBm, Pulsed
- TX PAE: 43.7% @ Pin = 18 dBm, Pulsed
- Package Dimensions: 6×6×1.0 mm

Performance is typical at room temperature. Please reference electrical specification table and data plots for more details.



6 mm × 6 mm QFN package

Functional Block Diagram



Description

The FR100XQ3 is a multi-die front-end module(FEM) designed for 8.0-11 GHz X-Band applications. The FEM integrates limiter, low-noise amplifier, and power amplifier. Transmit power is 16 W saturated with 39.8-46.3% PAE and receiver noise figure is 1.61dB. Receiver small signal gain is 26.5 dB, and transmitter large signal gain is 24.1 dB.

Applications

- Electronics Warfare (EW)
- Commercial and Military Radar
- Communications

DC Characteristics

PARAMETER	SYMBOL	VALUE	UNIT
RX Drain Voltage	V_{DD}	1.8	V
RX Drain Quiescent Current	I_{DDIDQ}	90	mA
RX Gate Control	V_{GG}	-1.7	V
TX Drain Voltage	V_D	24	V
TX Drain Quiescent Current	I_{DDIDQ}	210	mA
TX Gate Voltage	V_G	-1.93	V
Operating Temperature Range		-40 to 85	°C

1. Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

2. Gate voltage shown are typical, can be adjusted to set required drain current.

3. Control Voltages can use down to -10 V.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN VALUE	MAX VALUE	UNIT
PA Drain Voltage	V_D	-	29.5	V
PA Drain Current	I_{DDIDQ}	-	2000	mA
PA Gate Voltage	V_G	-5	0	V
PA Gate Current		-	10	mA
LNA Drain Voltage	V_{DD}	-	4.5	V
LNA Drain Current	I_{DDIDQ}	-	200	mA
LNA Gate Voltage	V_{GG}	-1.3	0	V
LNA Gate Current		-	10	mA
TX Input Power(@ 85°C, Pulse, 50 Ohm)		-	26	dBm
Mounting Temperature		-55	150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

Electrical Specifications, Receive

Test conditions unless otherwise noted: VDD = 1.8 V, IDDIDQ = 90 mA, CW

Data de-embedded to device reference plane, 25 °C.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Frequency	f	8.0		11	GHz
Small signal gain	G		26.5		dB
Noise Figure	NF		1.61		dB
Input Return Loss	IRL		25.3		dB
Output return loss	ORL		23.0		dB
Output P1dB*	P1dB		13.4		dBm
Output TOI @ -25 dBm Pin/Tone	OTOI		20.4		dBm

Electrical Specifications, Transmit

Test conditions unless otherwise noted: VDD = 24 V, IDIDQ = 210 mA

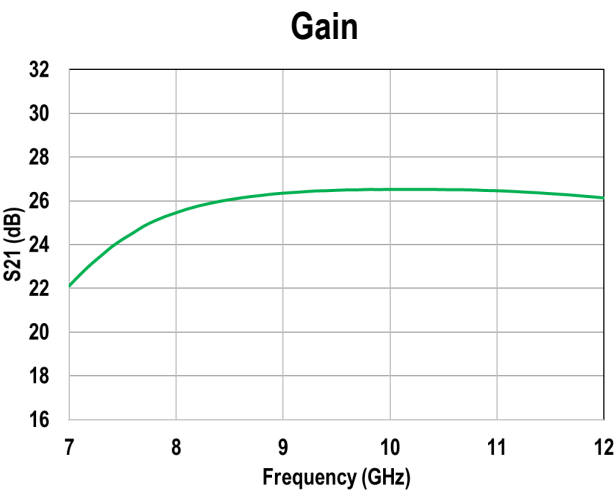
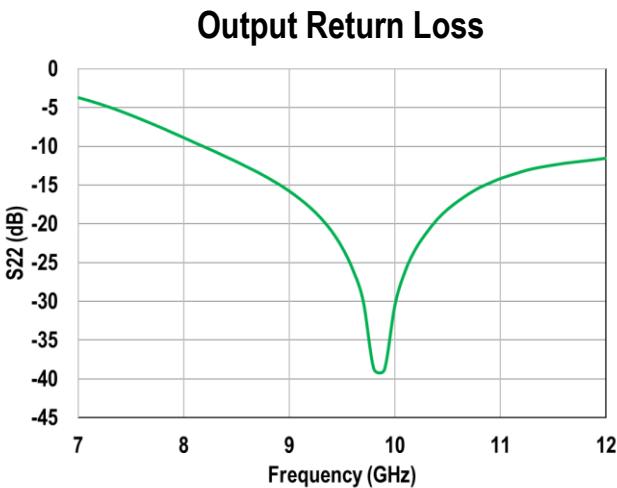
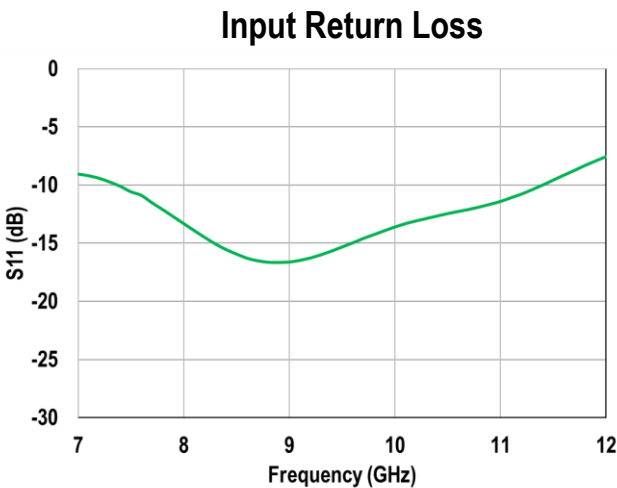
Data de-embedded to device reference plane, 25 °C.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Frequency	f	8.0		11	GHz
Small signal gain	G		34.8		dB
Large Signal Gain*	LG		24.2		dB
Input Return Loss	IRL		17.2		dB
Output return loss	ORL		12.2		dB
Output Power*	Psat		42.2		dBm
PAE	PAE		43.6		%

*Pin = 18 dBm, PW 100 μ s / DC 10% pulsed CW signal

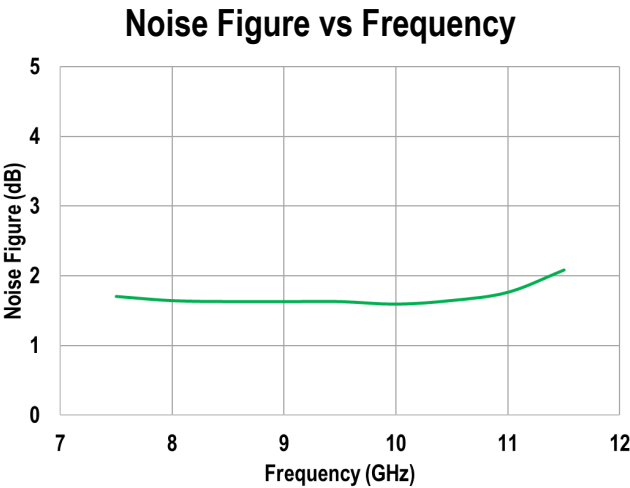
Small Signal Performance, Receive

Test Conditions unless otherwise stated: VDD = 1.8 V, IDDDIQ = 90 mA, 25 °C



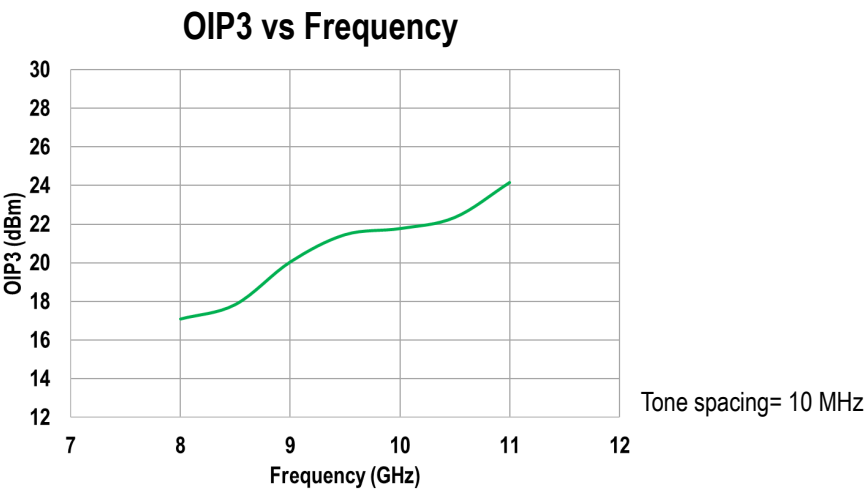
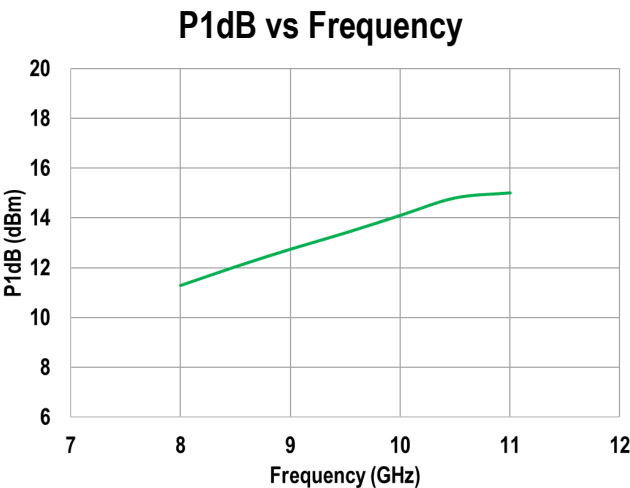
Noise Figure, Receive

Test Conditions unless otherwise stated: VDD = 1.8 V, IDDDIQ = 90 mA, 25 °C



Large Signal Performance, Receive

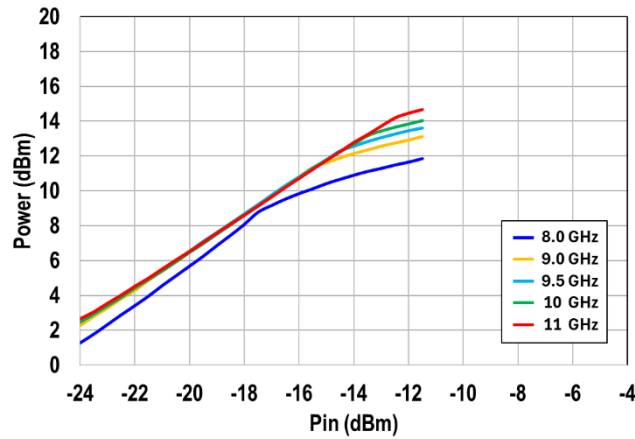
Test Conditions unless otherwise stated: VDD = 1.8 V, IDDDIQ = 90 mA, CW, 25 °C



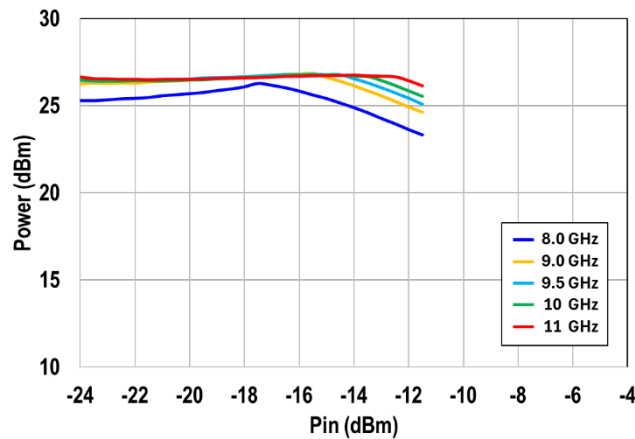
Power Sweep, Receive

Test Conditions unless otherwise stated: VDD = 1.8 V, IDDDIQ = 90 mA, CW, 25 °C

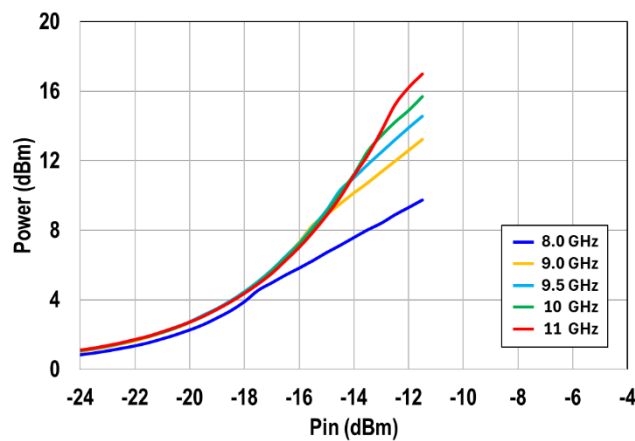
Power vs Pin



Power Gain vs Pin



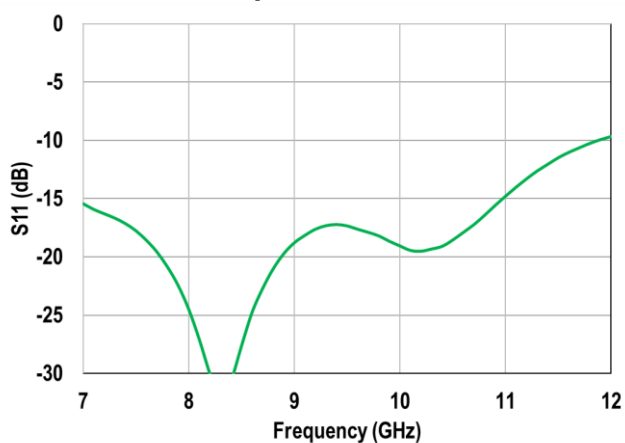
PAE vs Pin



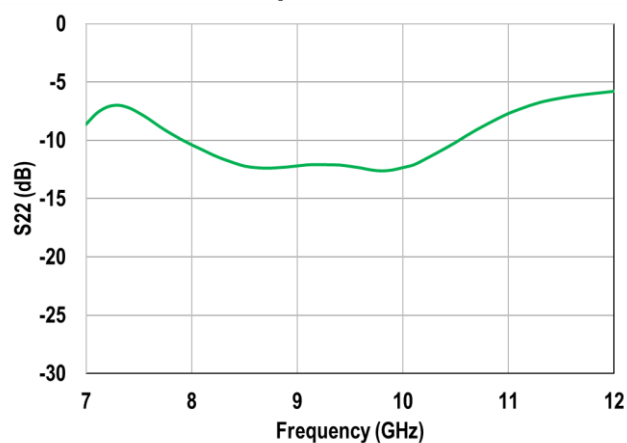
Small Signal Performance, Transmit

Test Conditions unless otherwise stated: $V_D = 24$ V, $I_{DIDQ} = 210$ mA, 25 °C

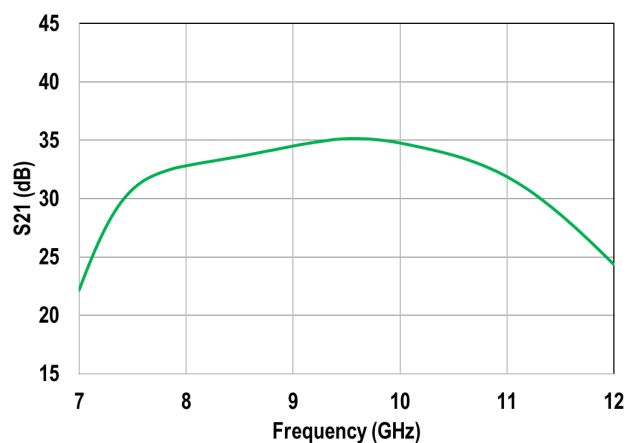
Input Return Loss



Output Return Loss



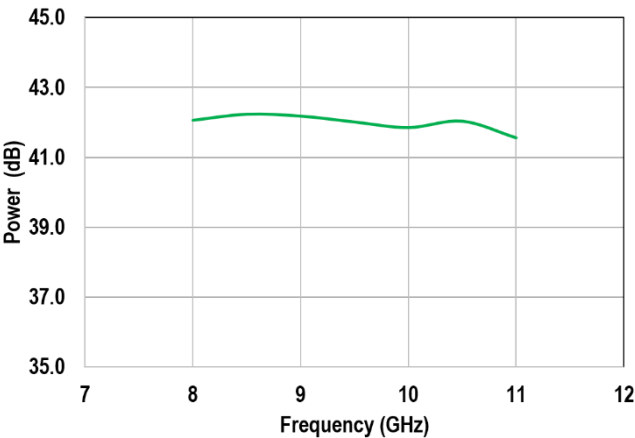
Gain



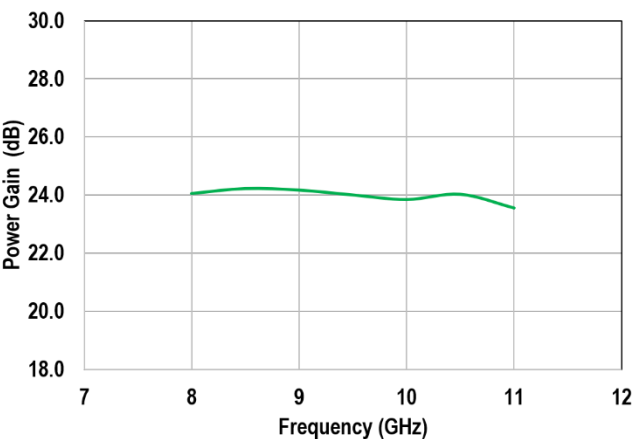
Large Signal Performance, Transmit

Test Conditions unless otherwise stated: $V_D = 24\text{ V}$, $I_{DIDQ} = 210\text{ mA}$
Pulse Mode, $P_{in} = 18\text{ dBm}$, $PW = 100\text{ }\mu\text{s}$, $DC = 10\%$, $25\text{ }^\circ\text{C}$

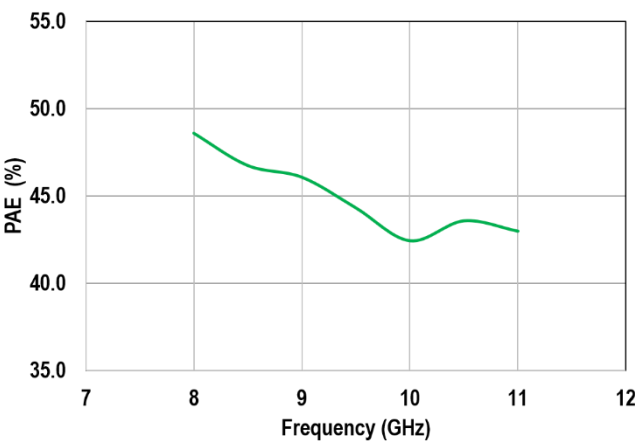
Power vs Frequency



Power Gain vs Frequency



PAE vs Frequency

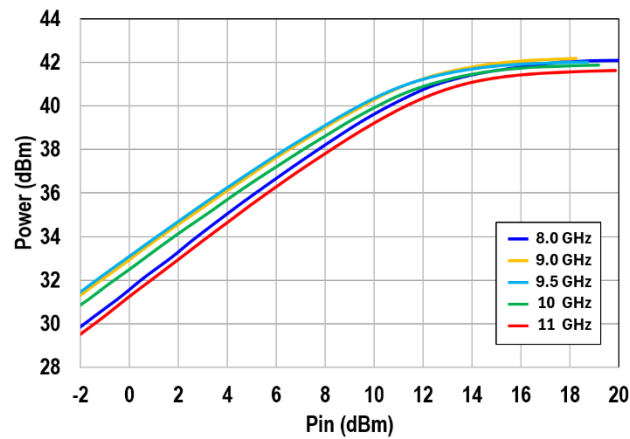


Power Sweep, Transmit

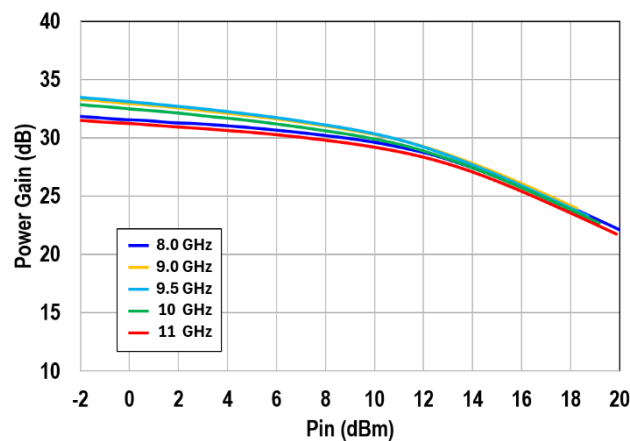
Test Conditions unless otherwise stated: $V_D = 24$ V, $I_{DIDQ} = 210$ mA

Pulse Mode, $PW = 100$ μ S, DC = 10%, 25 $^{\circ}$ C

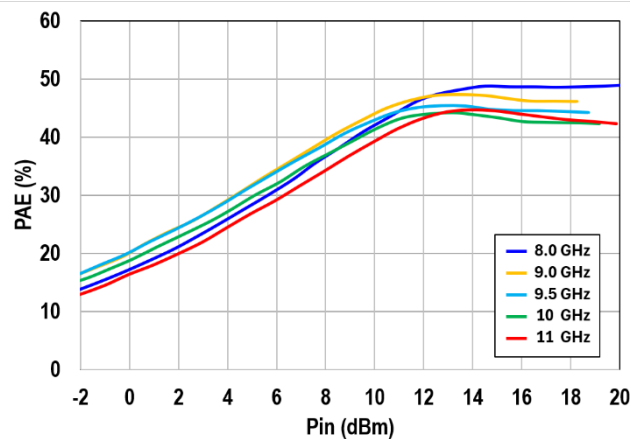
Power vs Pin



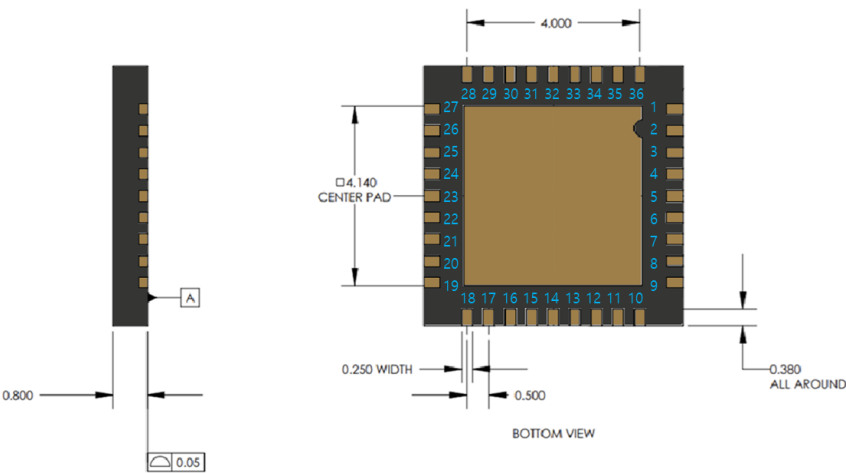
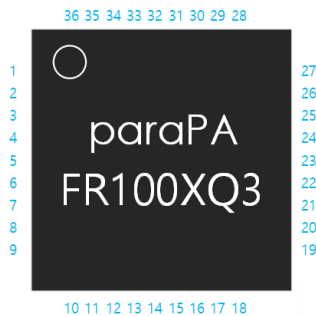
Power Gain vs Pin



PAE vs Pin



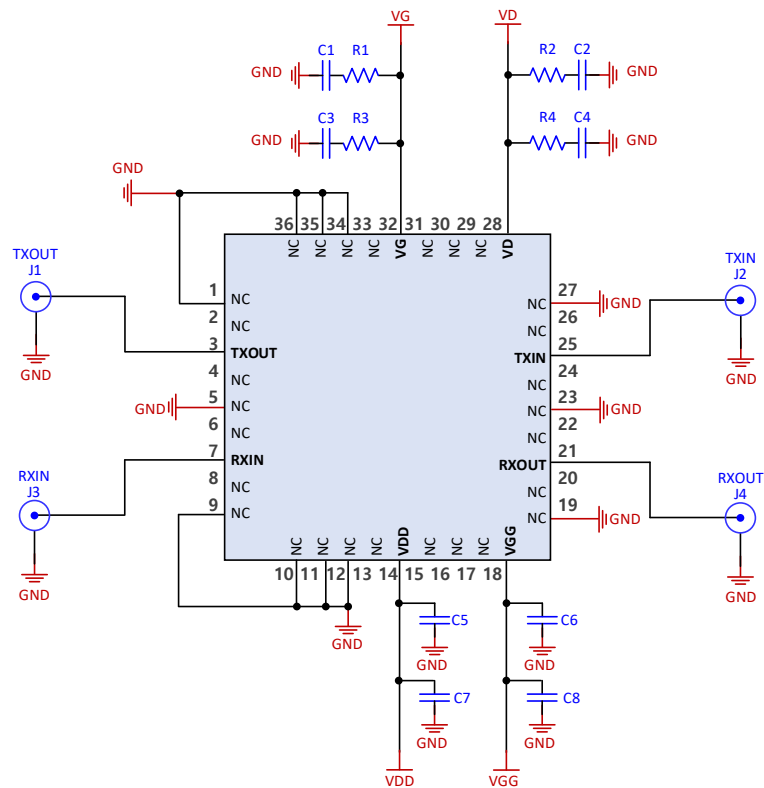
Mechanical Drawing & Pad Description



Dimensions in mm

Pin Number	Label	Description
Bottom Pad	GND	GROUND
3	TXOUT	Power Amplifier Output, DC Grounded
7	RXIN	Receive Input, DC Coupled
14	VDD	LNA Drain Supply
18	VGG	LNA Gate Control
21	RXOUT	Receive Output, DC Blocked
25	TXIN	Transmit Input, DC Blocked
28	VD	Transmit PA Drain Supply
29	VG	Transmit PA Gate Control
1-2, 4-6, 8-13, 15-17, 19-20, 22-24, 26-27, 30-36	N/C	No Internal Connections

Application Circuit



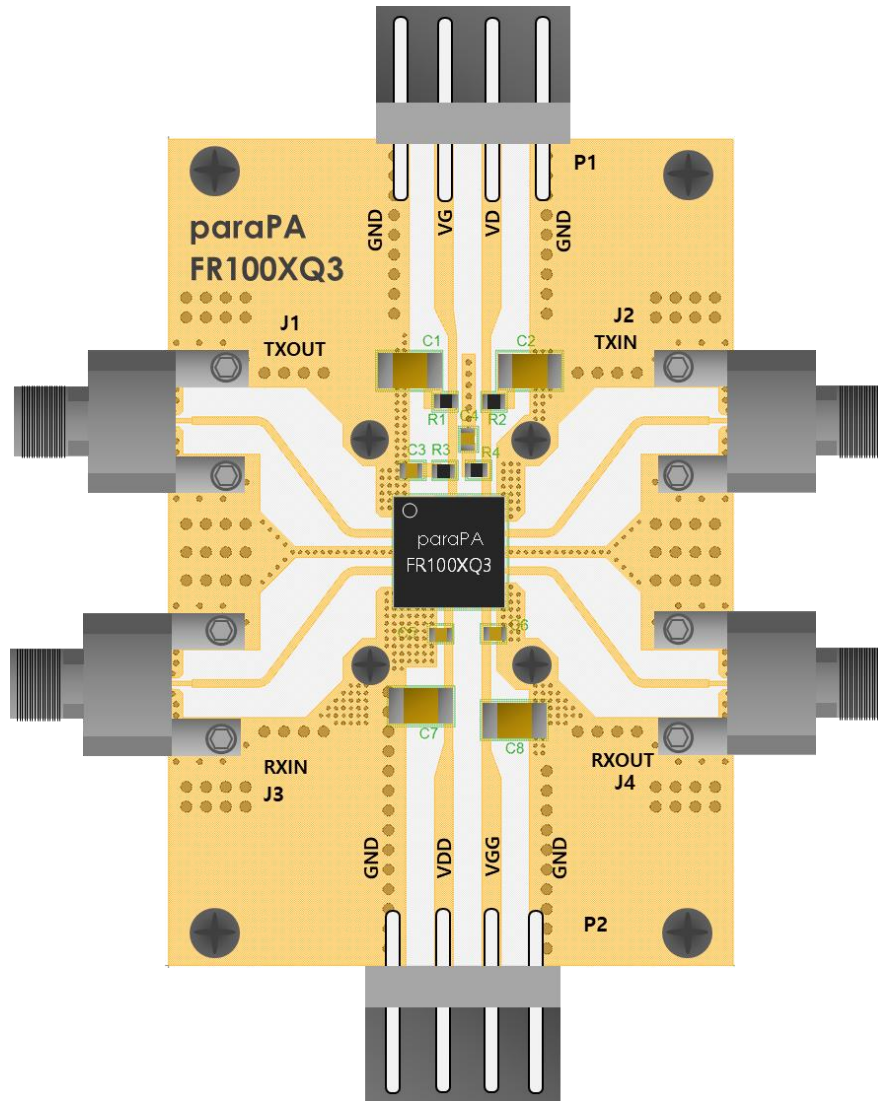
Bias-up Procedure

1. Set VD current limit to 2000 mA, VDD current limit to 200 mA, gate current limit to 10 mA
2. Set VGG to -3 V and VG to -5 V
3. Set VDD = +1.8 V, VD = +24 V
4. Adjust VG, VGG to achieve required drain current for TX (-1.9 V typical) and RX (-0.73 V typical)
5. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Set VGG = -3 V, VG to -5 V
3. Set VDD = 0 V, VD = 0 V
4. Turn off drain supply
5. Turn off gate supply

FR100XQ3 Evaluation Board



RF Layer is 0.008" thick Rogers Corp. RO4003C ($\epsilon_r = 3.35$). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the With-wave end launch connector NE02FS001.

Ref. Des.	Component	Value	Manuf.	Part Number
C1, C2, C7, C8	SMT Cap.	10 μ F, 1206 size, 10%, X5R, 50 V	Various	
C3, C4, C5, C6	SMT Cap.	0.1 μ F, 0402 size, 10%, X7R, 50 V	Various	
R1, R2	SMT Res.	0 Ohm, 0402 size, 0.1 W, 50 V	Various	
R3, R4	SMT Res.	5.1 Ohm, 0402 size, 1%, 0.625 W, 50 V	Various	
J1, J2, J3, J4	RF Connectors		With-wave	NE02FS001

Electrostatic Discharge (ESD) Classifications

PARAMETER	SYMBOL	CLASS	TEST METHODOLOGY
Human body model	HBM	TBD	TBD
Charge device model	CDM	TBD	TBD

For more information, please contact:

85517, Research Business Center
2066 Seobu-ro
Jangan-gu, Suwon-si, Gyeonggi-do, Korea
www.para-pa.com

Sales Contact
sales@para-pa.com